ISSUE 3 June 1995

1.0 Introduction

The following paragraphs describe a T1 trunk interface that meets the requirements of ANSI recommendation T1.403 using Mitel components and a low cost Channel Service Unit (CSU) or Office Repeater (OR).

This design establishes the performance monitoring and maintenance functions in the customer's equipment rather than in an external CSU, which provides the following benefits:

1) the Local Carrier interface can be a low cost CSU or OR, which will result in substantial cost savings for the end user, and

2) the customer can have access to performance data and maintenance functions.

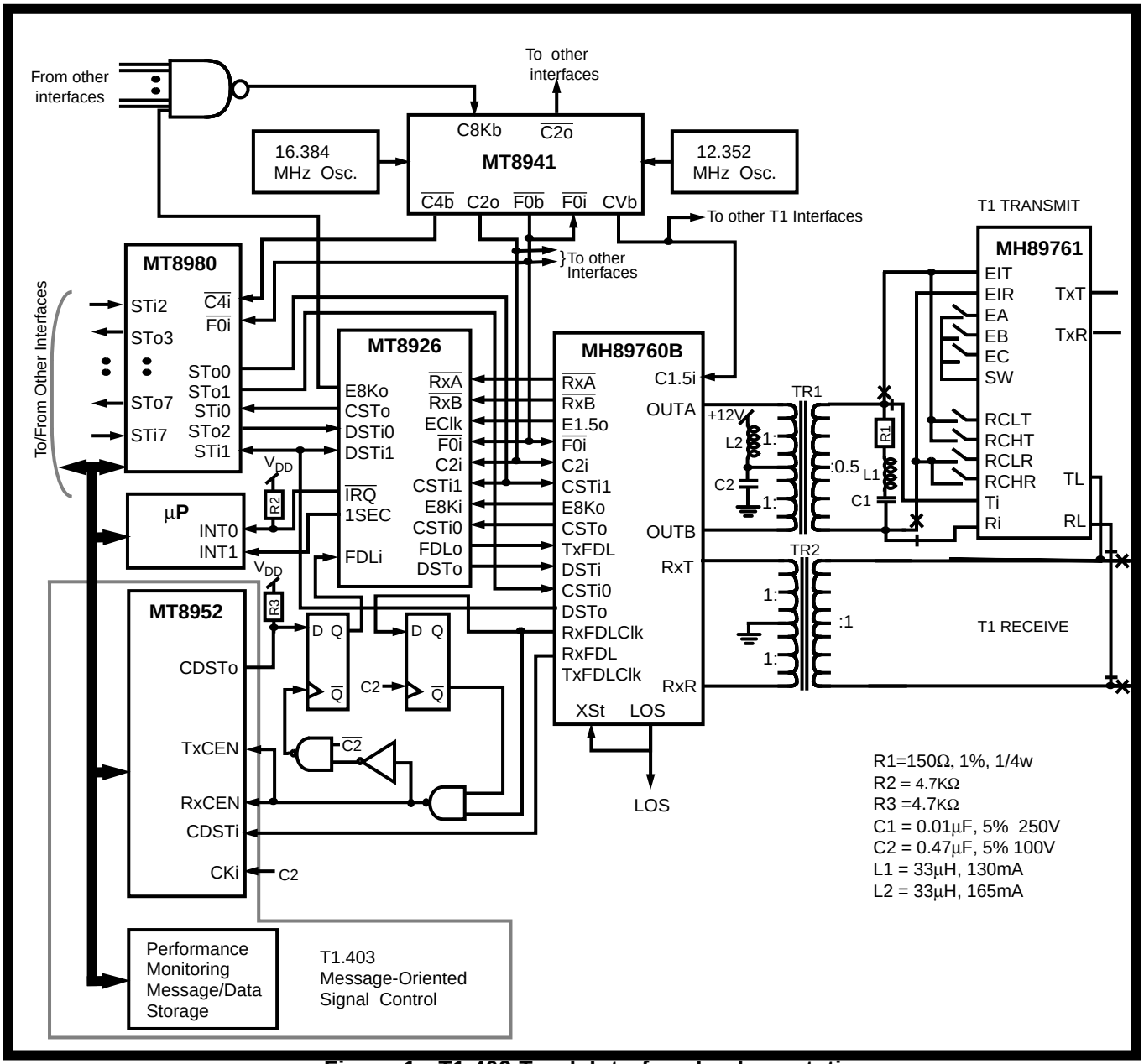

Figure 1 - T1.403 Trunk Interface Implementation

2.0 T1.403 Requirements

ANSI specification T1.403 entitled "Carrier-to-Customer Installation - DS1 Metallic Interface", states the physical layer, maintenance, performance monitoring and reporting requirements of a customer premises T1 interface. The following sub-sections briefly outline these requirements.

2.1 Physical Layer Requirements

T1.403 supplements the physical layer requirements of ANSI T1.102 to include the following:

- SF and ESF framing requirements (CRC-6 and Facility Data Link (FDL)).
- Electrical, jitter and connector requirements.
- Typical interface cable characteristics.

2.2 Maintenance Requirements

T1.403 includes the following maintenance requirements:

- SF and ESF Yellow alarm operation.
- Blue or AIS alarm operation.
- Loss of Signal indication.
- SF line loopback activate and deactivate code functions, as well as ESF line and payload loopback operation.

2.3 Performance Monitoring

The following transmission-error events are to be recorded as per T1.403:

- CRC-6 error event. Occurs when the locally generated CRC-6 remainder does not match the CRC-6 remainder received from the far end.
- Severely errored framing event. Occurs when two or more framing bit errors appear during a 3 msec. period.
- Frame-synchronization-bit error event. Occurs when a framing bit is received in error.
- Line-code violation event (BPVs). Occurs when the received line code does not match the selected AMI or B8ZS line encoding format.
- Controlled slips. Occurs when there is a replication or deletion of the DS1 frame by the received interface.

2.4 Performance Reporting

ANSI T1.403 defines an ESF mode Facility Data Link (FDL), which is used to transport performance information and control signals across a T1 link. The FDL channel is formed from the framing bit position of every second frame, and therefore, has a 4 Kbps bandwidth.

Two basic message formats have been defined for data and information transport across the FDL. These are Message-oriented performance reports (LAPD) and Bit-oriented messages (repeated 16 bit codewords).

The LAPD message-oriented performance reports are sent across the FDL once per second using the bit-assigned message structure described in T1.403. Every report contains performance data for each second of the previous four seconds.

Bit-oriented messages (BOMs) can preempt message-oriented reports, and consist of 16 bit codewords of the form 11111111 0XXXXXX0. This provides a maximum of 64 unique codewords or messages defined by XXXXXX. Refer to T1.403 for a list of messages and message restrictions.

BOMs are further divided into priority messages, and command and response messages. Priority messages indicate the existence of a service-affecting failure, and are repeated until the condition that initiated the message is removed. These BOMs are transmitted for at least one second, but may be interrupted as often as once per second, for a maximum of 100 msec. This is to accommodate the periodic transmission of message-oriented performance reports.

Command and response messages are used to perform line and payload loopbacks, protection switching, synchronization control, as well as other network functions. Each message consists of a 16 bit codeword of the form 11111111 0XXXXXX0, which is repeated at least 10 times.

User defined Operations, Administration and Maintenance (OA&M), terminal-to-network and terminal-to-terminal communications may also pass over the FDL.

3.0 Circuit Realization

Figure 1 illustrates the implementation of the T1.403 interface. The MH89760B provides the DS1 framer and line interface unit functions (see also the MH89761 T1 Transmit Equalizer data sheet). The MT8926 PMAC supplements the MH89760B by providing the required performance monitoring and maintenance functions. This is accomplished by connecting the PMAC to $\overline{\text{RxA}}$, $\overline{\text{RxB}}$ and the extracted clock (E1.5o) of the MH89760B, which allows it to receive FDL messages and analyse the received signal.

Both devices are ST-BUS compatible and use the same control streams. That is, the PMAC is programmed through the unused channels of the MH89760B's CSTi1 stream, and it will insert its data into the MH89760B's CSTo stream. See the MT8926 PMAC data sheet for more details.

The MT8941 is a dual DPLL that synchronizes the 2.048 MHz transmit clock (C2i) to the 1.544 MHz extracted network clock (E1.5o). The MT8952 HDLC device is used to transmit and receive performance messages across the 4 kbps FDL. The MT8980 is used in message mode to interface the microprocessor control and status bytes to ST-BUS format. It is also used to switch individual channels of the DSTi and DSTo streams.

3.1 MH89760B T1 Interface

The MH89760B is an upgraded pin-for-pin compatible version of the MH89760 bidirectional T1 interface, which includes a line interface unit, DS1 framer and slip buffer. MH89760B enhancements are inductorless receive clock recovery, internal RxD generation and Loss of Signal Indication (LOS).

3.2 MT8926 Performance Monitoring Adjunct Circuit (PMAC)

The MT8926 PMAC is an adjunct to the MH89760B that collects and reports the performance data specified in T1.403. This device has the following features:

- SF (D3/D4), and ESF modes of operation.
- One and two second timers for T1.403 message transmission.
- ESF and SF Yellow Alarms, Alarm Indication Signal (AIS), and Loss of Signal Indication (LOS).
- ESF Payload Loopback, and SF Line Loopback code generation and detection (integration).
- Supports bit-oriented and message-oriented data transfer over the Facility Data Link (FDL).
- Framing Error, Severely Errored Farming Event, CRC Error, and Bipolar Violation Error Counters.
- Alarm interrupts and counter overflow interrupts.

3.3 Circuit Description

A Loss of Signal (LOS) indication function exists in both the MT8926 and MH89760B. The MH89760B LOS is a physical output and has been wired to the status input (XSt) in Figure 1. The PMAC indicates a LOS condition by bringing the LOS bit high in master status word one.

DSTo of the MH89760B passes through the MT8926 to allow the implementation of an ESF payload loopback. The PMAC will also decode and transmit SF line loopback activation and deactivation codes. The line loopback is implemented by activating the MH89760B remote loopback.

The PMAC has Bit-oriented Message registers (BOMs) that allow it to transmit and receive (decode) bit-oriented messages. When a message is decoded a valid message indication is provided to the microprocessor via the ST-BUS and MT8980. Transmit message-oriented communication is supported by muxing the FDL data source from the PMAC BOM register to its FDLi input, which connects to CDSTo of the MT8952 HDLC controller in Figure 1. See section 2.4 for an explanation of performance reporting messages.

The RxFDL output of the MH89760B is connected to CDSTi of the MT8952 to support the reception of LAPD message-oriented signals. The MT8952 will identify a message-oriented signal by the opening and closing flags (01111110) of the message. Therefore, this bit sequence should not be used as a bit-oriented message (0XXXXXX0). The MT8952 will recognize the 11111111 bit-oriented message preamble as an abort signal, so these messages can preempt message-oriented signals.

The MT8952 interrupts are generated using the CKi clock input. Therefore, glue circuitry has been added to the MH89760B to MT8952 interface, which allows the MT8952 CKi input to be clocked by $\overline{\text{C2}}$ (2.048 MHz) instead of RxFDLCLK (4 kHz).

The MH89760B extracted clock (E8Ko) is used by the PMAC (E8Ki) to align the device to the received signal. The network timing source is selected

through the PMAC E8Ko rather than the MH89760B E8Ko.

The PMAC signals $\overline{IRQ}$ and 1SEC are implemented as microprocessor interrupt sources. $\overline{IRQ}$ will be pulled low by the PMAC when an exception condition or a counter overflow occurs. The 1SEC interrupt can be used to signal the microprocessor to transmit a periodic message-oriented LAPD packet to the network.

The Microprocessor block of Figure 1 controls the ST-BUS devices through the MT8980 in message mode. The MT8952 and RAM are controlled via the microprocessor address/control/data bus.

4.0 Software Requirements

The T1.403 interface of Figure 1 will require the implementation of the following software functions:

- The basic device drivers for the MH89760B/ MT8926, MT8980 and MT8952.
- Performance monitoring software that will read the performance data from the PMAC and store it in RAM in T1.403 message-oriented signal format.
- An interrupt service routine that will initiate transmission of the current message-oriented packet.
- Bit-oriented message control and response software.
- Control software that allows the interworking of message-oriented and bit-oriented signals.